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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,641	10/09/2003	Dwight W. Mattix	030393	1207

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QUALCOMM INCORPORATED
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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	PAPER NUMBER
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/683,641	MATTIX, DWIGHT W.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,12-21 and 23-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-21 and 23-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 November 2006 has been entered.

Claim Rejections - 35 USC § 102

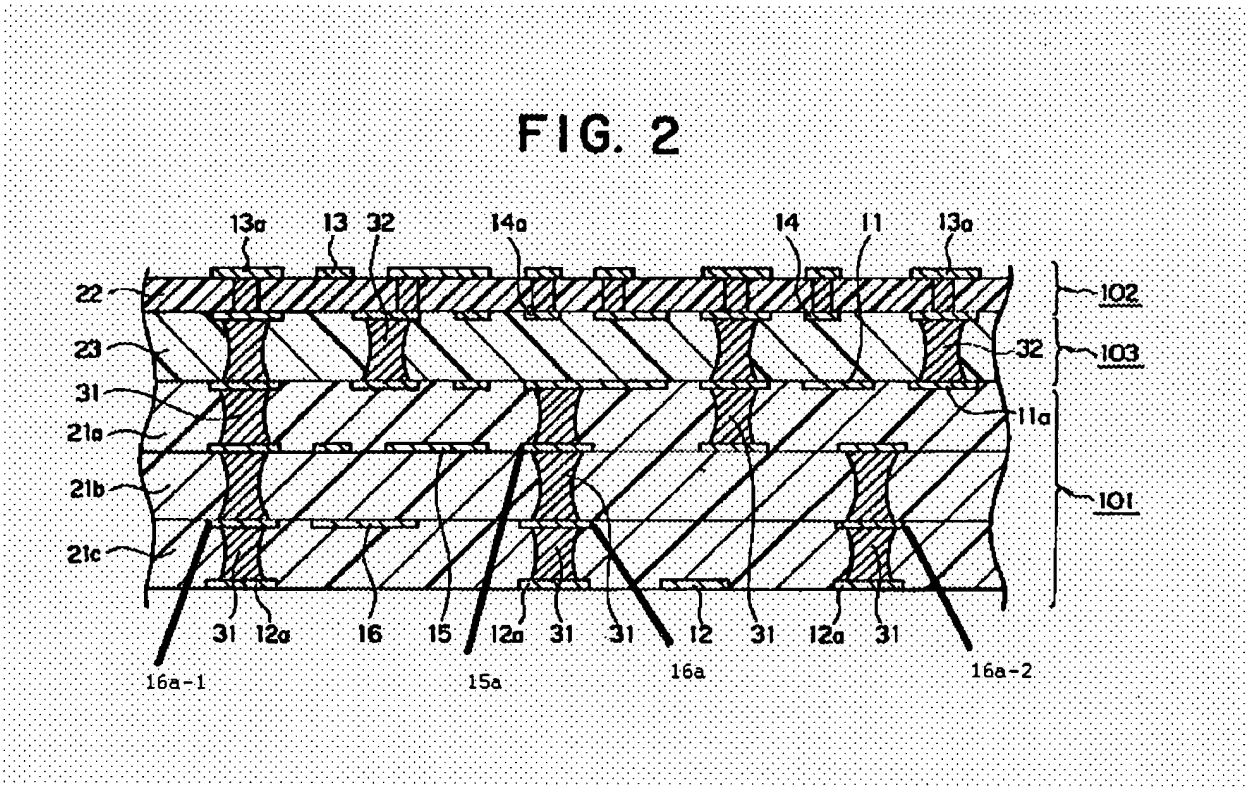
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 8, 18-21, and 23-57 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,329,610 (Takubo).

An annotated version of figure 2 of Takubo is included herein below to assist in explanation.

FIG. 2



Takubo discloses, referring primarily to figure 2, an interlayer interconnection unit for a printed circuit board (PCB), comprising: an interstitial bridge pad (16a) having a first side (top side as viewed in figure 2) and a second side (bottom side as viewed in figure 2), wherein said first side of said interstitial bridge pad physically contacts a first dielectric layer (21b) and said second side of said interstitial bridge pad physically contacts a second dielectric layer (21c); a first blind via (31) disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer and a second blind via (31) disposed on said second side of said interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via, wherein said interstitial bridge pad is coaxial in a z

direction with said first blind via and with said second blind via (see figure 2), and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 1**], wherein said interstitial bridge pad comprises a disc-shaped conductive element (col. 16, lines 30-45) [**claim 2**] wherein said first blind via extends from a first conductive layer (15a), through said first dielectric layer, and to said first side of said interstitial bridge pad, and said second blind via extends from a second conductive layer (12a), through said second dielectric layer; and to said second side of said interstitial bridge pad [**claim 3**], wherein said first conductive layer and said second conductive layer each comprise copper foil (col. 15, lines 45-55) [**claim 4**], wherein said first blind via extends from a first capture pad (15a) to said first side of said interstitial bridge pad, and said second blind via extends from a second capture pad (12a) to said second side of said interstitial bridge pad [**claim 5**], wherein said interstitial bridge pad has a diameter in the range of from about 12 to 20 mils (col. 16, lines 30-45) [**claim 7**], wherein: said PCB comprises a bridge layer (16) disposed between said first dielectric layer and said second dielectric layer, and said interstitial bridge pad is located within said bridge layer, and wherein said interstitial bridge pad lacks electrical connection, within said bridge layer, to a conductive element of said bridge layer [**claim 8**].

Similarly, Takubo discloses, a dual blind via interconnection unit for a multilayer PCB, comprising: a pair of opposed coaxial blind vias (31, 31) transversing a pair of dielectric layers (21b, 21c); and at least one bridge pad (16a) disposed between said pair of dielectric layers, wherein each of said pair of blind vias is in contact with said

bridge pad and wherein said bridge pad is adapted to electrically interconnect said pair of opposed coaxial blind vias without electrically interconnecting any other blind vias, wherein a first bridge pad of said at least one bridge pad lacks electrical connectivity to others of said at least one bridge pads [**claim 18**], wherein the bridge pad has a diameter in the range from about 12-20 mils (col. 16, lines 30-45) [**claim 19**], wherein each of said pair of blind vias has a diameter in the range from about 4 to 6 mils (col. 16, lines 30-45) [**claim 20**].

Also, Takubo discloses, a carrier for a multilayer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including: a first metal layer (15); a first dielectric layer (21b) disposed on said first metal layer; a bridge layer (16) disposed on said first dielectric layer; a second dielectric layer (21c) disposed on said bridge layer; and a second metal layer (12) disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads (16a, 16a-1, 16a-2), and wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said first metal layer by a first blind via (31) transversing said first dielectric layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said second metal layer by a second blind via (31) transversing said second dielectric layer, and wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 2), and wherein, in the absence of an interstitial bridge pad

therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 21**], wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads [**claim 23**], wherein said plurality of interstitial bridge pads are spaced apart from each other by a distance in the ranges of from about 0.7 to 4 mils (col. 16, lines 30-45) [**claim 24**], wherein the plurality of interstitial bridge pads are arranged within said bridge layer at a center to center pitch in the range of from about 15 to 25 mils (col. 16, lines 30-45) [**claim 25**], wherein said first metal layer comprises a first signal layer of said PCB, and said second metal layer comprises a second signal layer of said PCB [**claim 26**], further comprising at least a third signal layer (11) laminated to said pseudo three-layer core [**claim 27**], wherein said carrier comprises from 2 to 4 additional layers (11, 14) laminated to said pseudo three-layer core [**claim 28**].

Moreover, Takubo discloses, a pseudo three-layer core for a printed circuit board (PCB), comprising: a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer (15) to a second metal layer (12); a first dielectric layer (21b) disposed on said first metal layer; a bridge layer (16) disposed on said first dielectric layer; and a second dielectric layer (21c) disposed on said bridge layer, wherein said second metal layer is disposed on said second dielectric layer, and wherein at least one of said plurality of interlayer interconnection units comprises: an interstitial bridge pad (16a) located within said bridge layer; a first blind via (31) extending from said first metal layer to a first side of said interstitial bridge pad; and a second blind via (31) extending from said second

metal layer to a second side of said interstitial bridge pad, and wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 2), and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 29**]

Furthermore, Takubo discloses a multi-layer printed circuit board (PCB), comprising: a first signal layer (15); a second signal layer (12) a bridge layer (16) disposed between said first signal layer and said second signal layer; and a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer interconnection units comprises: a pair of opposed coaxial blind vias (31, 31) transversing a first dielectric layer (21b) and a second dielectric layer (21c); and a bridge pad (16a) physically contacting said first and second dielectric layers, said bridge pad in electrical contact with said pair of blind vias, and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 30**], wherein: said bridge pad includes a first side and a second side; and wherein said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad [**claim 31**], further comprising at least one additional dielectric layer (21a) laminated to said first signal layer, and at least one

additional signal layer (11a) laminated to said at least one additional dielectric layer [**claim 32**].

Moreover, Takubo discloses, a multi-layer PCB, comprising: at least one pseudo three-layer core including: a first metal layer (15); a first dielectric layer (21b) disposed on said first metal layer; a bridge layer (16) disposed on said first dielectric layer; a second dielectric layer (21c) disposed on said bridge layer; a second metal layer (12) disposed on said second dielectric layer; and a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises: an interstitial bridge pad (16a) having a first side and a second side; a first blind via (31) disposed on said first side of said interstitial bridge pad extending through said second dielectric layer, and a second blind via (31) disposed on said second side of said bridge pad extending through said second dielectric layer, and wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 2), and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 33**], wherein each of said plurality of interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer [**claim 34**], wherein each of said first metal layer and said second metal layer comprises a signal layer and said multilayer PCB further comprises at least one additional signal layer (11) laminated to said at least one pseudo three-layer core [**claim 35**], wherein said at least one pseudo three-layer core comprises a first pseudo three-

layer (12, 16, 15) core and at least a second pseudo three-layer (11, 14, 13) core laminated to the first pseudo three-layer core [**claim 36**] wherein said multilayer PCB comprises 1 pseudo three-layer core and 4 signal layers (12, 15, 11, 14) [**claim 37**].

Additionally, Takubo discloses, a multilayer PCB, comprising: means for carrying a plurality of signal layers; and means for interconnecting at least two of said plurality of signal layers, wherein said carrying means comprises a pseudo three-layer core, wherein said pseudo three-layer core includes an internal bridge layer (16) that comprises a plurality of interstitial bridge pads (16a, 16a-1, 16a-2), a first dielectric layer (21b), and a second dielectric layer (21c) and wherein said interconnecting means comprises a pair of opposed blind vias (31, 31) disposed on either side of each of said plurality of interstitial bridge pads said pair of opposed blind vias transversing said first and second dielectric layers and, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 2), and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 38**], wherein said bridge layer comprises an internal pseudo metal layer (106a) disposed between a first dielectric layer (101) and a second dielectric layer (103), and wherein said interconnecting means is adapted for interconnecting said plurality of signal layers [**claim 39**].

In addition, Takubo discloses a method for forming a multilayer printed circuit board (PCB), comprising: a) providing a metal clad first dielectric layer (21b) having first metal clad side and a second metal clad side, b) forming a bridge layer (16) from said

second metal clad side, wherein said bridge layer comprises a plurality of bridge pads (16a, 16a-1, 16a-2) disposed on said first dielectric layer, and wherein said first metal clad side comprises a first metal layer (15); c) providing a second dielectric layer (21c) on said bridge layer, wherein said second dielectric layer has a second metal layer (12) disposed thereon; d) forming a first blind via (31) through said first dielectric layer, wherein said first blind via extends from said first metal layer to a first side of at least one of said plurality of bridge pads; and e) forming a second blind via (31) through said second dielectric layer, wherein said second blind via extends from said second metal layer to a second side of said at least one of said plurality of bridge pads [**claim 40**], wherein said step b) comprises etching said second metal clad side of said first dielectric layer to form said at least one of said plurality of bridge pads (col. 21, lines 10-15) [**claim 41**], wherein: said second metal clad side comprises copper foil, and wherein said at least one of said plurality of bridge pads comprises copper (col. 21, lines 10-15) [**claim 42**], wherein each of said plurality of bridge pads has a diameter in the range from about 12 to 20 mils (col. 16, lines 30-45) [**claim 43**], wherein said bridge layer lacks electrical connectivity between said plurality of bridge pads [**claim 44**], wherein said steps c) and d) respectively comprise forming said first blind via and said second blind via by a process selected from the group consisting of laser drilling, plasma drilling, and photo-defining (col. 22, lines 5-25) [**claim 45**], further comprising: e) plating shut said first blind via and said second blind via (col. 26, lines 55-65) [**claim 46**], wherein said method involves only a single plating cycle [**claim 47**], wherein after said step e), said first metal layer and said second metal layer each have a thickness in the

range of from about 0.8 to 1.4 mils (col. 22, lines 10-15) [**claim 48**], wherein after said step e) said first metal layer and said second metal layer each have a thickness in the range of from about 0.9 to 1.1 mils (col. 22, lines 10-15) [**claim 49**], wherein said first blind via and said second blind via each comprise a μvia having a diameter in the range from about 4-5 mils (col. 16, lines 30-45) [**claim 50**].

Moreover, Takubo discloses, a method for forming a multilayer printed circuited board (PCB), comprising: a) forming a pseudo three-layer core, said pseudo three-layer core including: a first metal layer (15); a first dielectric layer (21b) disposed on said first metal layer, a plurality of spaced apart interstitial bridge pads (16a, 16a-1, 16a-2) disposed on said first dielectric layer; a second dielectric layer (21c) disposed on said plurality of spaced apart interstitial bridge pads; and a second metal layer (12) disposed on said second dielectric layer, and b) forming a plurality of interlayer interconnection units for interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes: a first blind via (31) disposed on a first side of one of said plurality of interstitial bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and a second blind via (31) disposed on a second side of one of said plurality of interstitial bridge pads, wherein said second blind via (31) extends from said second metal layer through said second dielectric layer wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 2) [**claim 51**], wherein: said step b) comprises plating shut said first blind via and said second blind via, and said method includes only a single plating cycle (col. 26, lines 55-65) [**claim 52**], wherein

each of said first blind via and said second blind via has an aspect ratio of at least about 1:1 [**claim 53**], wherein each of said interlayer interconnection units has an effective aspect ratio of at least about 2:1 [**claim 54**].

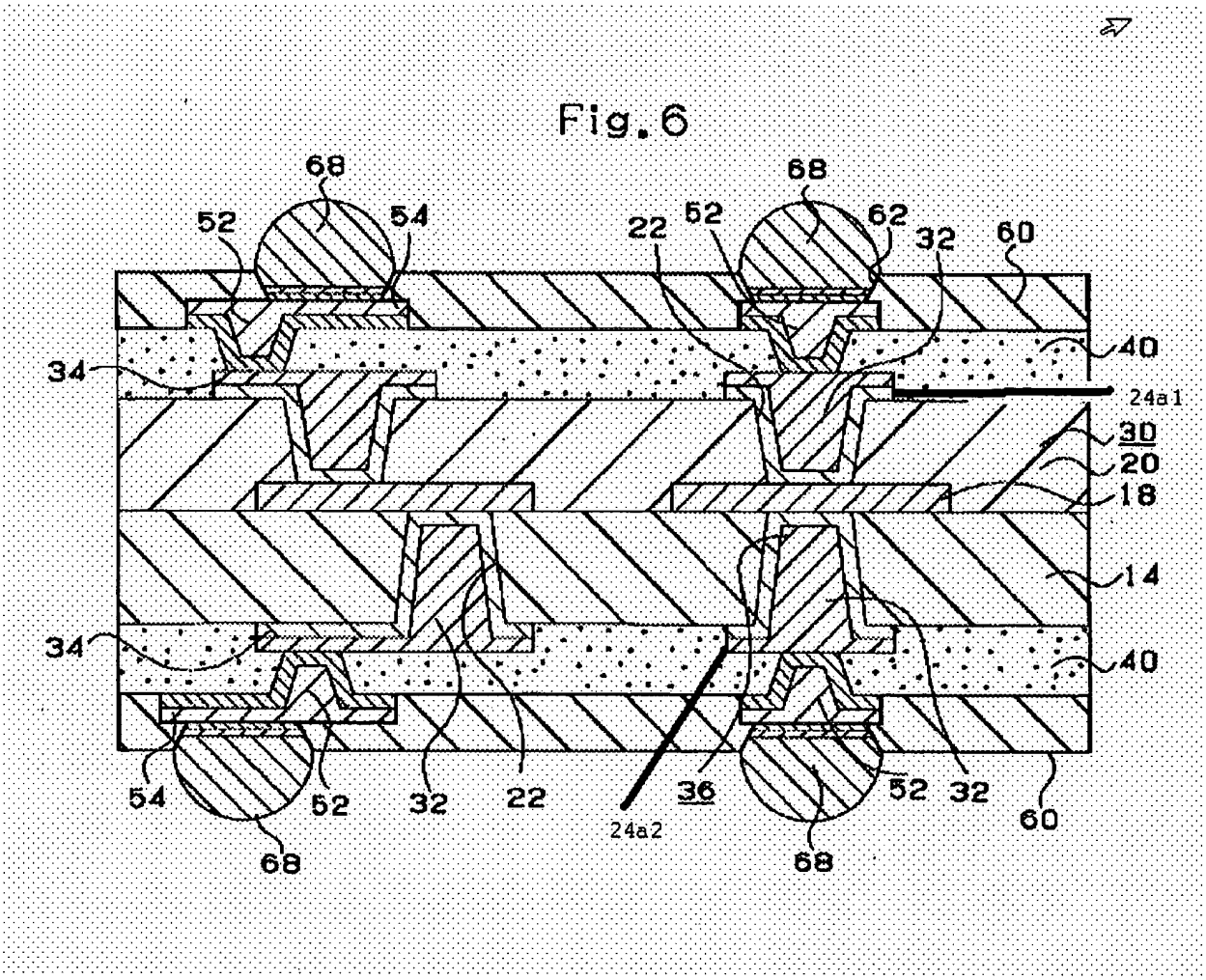
Alternately, Takubo discloses, referring primarily to figure 2, a method for forming a multilayer printed circuit board (PCB), comprising: a) a step for forming a pseudo three-layer core, wherein said pseudo three- layer core includes a first metal layer (12a), a first dielectric layer (21c) disposed on said first metal layer; a bridge layer (16) disposed on said first dielectric layer; a second dielectric layer (21b) disposed on said bridge layer; and a second metal layer (15) disposed on said second dielectric layer; and b) a step for forming a plurality of interlayer interconnection units for electrically interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes a pair of opposed coaxial blind vias (31), and one of said plurality of bridge pads disposed between, and in electrical contact with, said pair of blind vias [**claim 55**].

Similarly, Takubo discloses method for forming a pseudo three-layer core for a PCB, comprising: a) providing a first metal layer (15), b) providing a first dielectric layer (21b) on said first metal layer; c) forming a plurality of bridge pads (16a, 16a-1, 16a-2) on said first dielectric layer; d) providing a second dielectric layer (21b) on said plurality of bridge pads; e) providing a second metal layer on said second dielectric layer; f) forming a first blind via (31) on a first side of each of said plurality of bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and g) forming a second blind via (31) on a second side of each of said plurality of

bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer wherein said each of said plurality of bridge pads is coaxial in a z direction with said first blind via and with said second blind via (see figure 2) [**claim 56**], wherein: said first dielectric layer comprises a first side and a second side, said first side having said first metal layer disposed thereon, and said second side having a layer of copper foil disposed thereon, and said step c) comprises etching said layer of copper foil (col. 22, lines 10-20) [**claim 57**].

Claims 1, 6, 10, and 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by US 2005/0039948 A1 (Asai).

An annotated version of figure 6 of Asai is included herein below to assist in explanation.



Asai discloses, referring primarily to figure 6, an interlayer interconnection unit for a printed circuit board (PCB), comprising: an interstitial bridge pad (18) having a first side (top side as viewed in figure 2) and a second side (bottom side as viewed in figure 2), wherein said first side of said interstitial bridge pad physically contacts a first dielectric layer (20) and said second side of said interstitial bridge pad physically contacts a second dielectric layer (14); a first blind via (22) disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer and a second blind via (22) disposed on said second side of said

interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via (see figure 6), and wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer [**claim 1**], wherein said first capture pad and said second capture pad each have a diameter less than a diameter of said interstitial bridge pad [**claim 6**].

Similarly, Asai discloses, referring primarily to figure 6, an interlayer interconnection unit for a multi-layer PCB, comprising: a first capture pad (24a1) having a first annular ring; a first via (22) having a first via inner end and a first via outer end, said first via outer end in contact with said first capture pad and encircled by said first annular ring; an interstitial bridge pad (18) having a first side and a second side, said first via inner end in contact with said first side of said interstitial bridge pad; a second via (22) having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said interstitial bridge pad; and a second capture pad (24a2) having a second annular ring, said second via outer end in contact with said second capture pad and encircled by said second annular ring, wherein a first interstitial bridge pad of said at least one interstitial bridge pad lacks electrical connectivity to others of said at least one interstitial bridge pads and wherein said first annular ring, said first via, said interstitial bridge pad said second via, and said second annular ring are coaxial with each other [**claim 10**] wherein said first via extends

through a first dielectric layer (20), and said second via extends through a second dielectric layer (14) [**claim 12**], wherein said interstitial bridge pad has a diameter in the range from about 14 to 17 mils ([0175]) [**claim 13**], wherein said multilayer PCB comprises an internal bridge layer (18), and said interstitial bridge pad is a component of said bridge layer [**claim 14**], wherein each of said first via and said, second via has an aspect ratio of at least about 1:1 (length = 300μm [0173]; diameter = 250μm [0175]; thus L:D is greater than 1:1) [**claim 15**], wherein said interconnection unit has an effective aspect ratio greater, than about 2:1 (length = 650μm [0173]-[0175]; diameter = 250μm [0175]; thus L:D is greater than 2:1) [**claim 16**], wherein: said first capture pad is located within a first conductive layer said second capture pad is located within a second conductive layer , and said interconnection unit further comprises a third via (52) extending from said first capture pad or said second capture pad to a third conductive layer [**claim 17**].

Response to Arguments

Applicant's arguments filed 08 November 2006 have been fully considered but they are not persuasive. Applicant alleges that the conductive feedthrough disclosed by Takubo "is not a blind via, but rather a **conductive pillar** piercing through a third insulation layer" (emphasis Applicant's) and that "Takubo specifically notes the difference between via holes and conductive pillars". However this is not well taken for at least three reasons. First, referring, for example to figure 3, Takubo discloses wiring patterns (11a) connected solely to conductive pillars (31, 32), yet refers to said wiring patterns as "via land" (col. 19, lines 55-60). Thus, it is readily apparent to the ordinarily

skilled artisan that the conductive pillars of Takubo are intended to be construed as "vias". Secondly, Applicant's contention that "Takubo specifically recites that the wiring layers 11, 12 may be connected with a conductive pillar or, alternatively with a via hole" is in error. Takubo actually states, "Alternatively, a layer connecting means such as a through-hole other than the conductive pillar may be used (col. 19, lines 1-5)". This is stressing the difference between a filled feedthrough such as the conductive pillar and a hollow feedthrough such as a through hole. The ordinarily skilled artisan would certainly not construe this teaching to exclude the conductive pillars from the realm of "vias". Lastly, even assuming *en arguendo* that the conductive pillars of Takubo are not "vias", clearly, Takubo discloses that through holes may be used in place of the conductive pillars (col. 19, lines 1-5). Thus there can be no argument that Takubo does not disclose such vias.

As for Applicant's argument that "the invention of Takubo requires **three insulation** layers" (emphasis Applicant's), this too is not well taken as 1) Applicant has dismissed the fact that the dielectric layer pierced by the conductive pillar is an insulating layer in its own right and thus can serve as the first insulation layer in the instantly claimed invention. Furthermore, since Applicant has opted to use open ended language (e.g. 'comprising') to define the claimed invention, applied Prior Art may have additional structure than that which is claimed. As detailed in the above rejection, the invention of Takubo does indeed disclose the first and second dielectric layers fused to one another in a portion other than where a bridge pad exists.

Regarding claims 51 and 55, Applicant alleges "these claims have been amended to clarify that the bridge layer consists of a plurality of interstitial bridge pads". However, this is not actually the case as the currently drafted and rejected version of these claims merely state the limitation "a plurality of spaced apart interstitial bridge pads", which does not preclude other additional structure. Indeed in each of the claims all reference to a "bridge layer" have been removed, so there cannot exist an exclusive limitation to something that is not even present in the claims.

Applicant's arguments with respect to claims 7, 10, 12-17, 19, 20, 24, 25, 43, and 50 have been considered but are moot in view of the new ground(s) of rejection.

Hence, Applicant's traversal of the instant rejections on these grounds is deemed unsuccessful.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Patent Examiner - Technology
Center 2800
Art Unit 2841

JCSN